

MR2707-3

Serial Number: 09/990,273

Reply to Office Action dated 10 January 2005

**AMENDMENTS TO THE SPECIFICATION**

**I. Please replace the paragraph beginning on page 4, line 23, and ending on page 6, line 5, with the following amended paragraph:**

FIG. [[1]] 2 shows the circuit block diagram of one embodiment according to the present invention, which comprises an integrated circuit 20 able to switch between ultrasonic and infrared carriers, and at least one set of infrared LIGHT EMITTING DIODE 40 or ultrasonic transducer 50. The integrated circuit 20 provides two carrier signal output ports OUT1 and OUT2 to output oscillating signals. Moreover, the integrated circuit 20 able to switch between ultrasonic and infrared carriers includes a frequency divider 24 where different divider can be set and circuit blocks 202 and 204. Carriers of different frequencies are obtained by dividing the oscillation frequency 22 by the frequency divider 24, and the circuit blocks 202 and 204 have the same architecture, which comprise multiplexers 30A and 30B, and output buffers 32A and 32B, respectively. The oscillation frequency 22 is divided by the frequency divider 24, then processed by the circuit block 202, and eventually outputted from the port OUT1. In the same manner, the oscillation frequency 22 is divided by the frequency divider 24, then processed by the circuit block 204, and eventually outputted from the port OUT2. For the first carrier signal output port OUT1, the carrier signal it outputs is obtained through the process that the frequency divider 24 divides the oscillation frequency 22 to produce the desired carrier, for instance a continuous carrier, and feeds it to the multiplexer 30A

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which has the other input to accept the user controlled signal ~~DATA-128A~~ DATA1 28A, and the output of the multiplexer 30A is sent to the first carrier signal output port OUT1 through the output buffer 32A so as to transmit the DATA. The process for the second carrier signal output port OUT2 is similar to that for the first carrier signal output port OUT1, only that the oscillation frequency 22 divided by the frequency divider 24 is further inverted by the inverter 26 before it is connected to the circuit block 204, and thus the carrier signal from the second carrier signal output port OUT2 has a phase opposite to that of the carrier signal from the first carrier signal output port OUT1.

**II. Please replace the two consecutive paragraphs beginning on page 6, line 13, and ending on page 7, line 14, with the following amended paragraphs:**

FIG. 3 shows a detail circuit schematic for implementation of the above embodiment. The multiplexer 30A comprises crystal oscillators and controls the output by use of a select control signal MODE1 34A. When the select control signal MODE1 34A is 0, the multiplexer 30A outputs data signal ~~DATA-128A~~ DATA1 28A. On the contrary, when the select control signal MODE1 34A is 1, the multiplexer 30A outputs a carrier FRE from the frequency divider 24. The output buffer 32A includes a digital logic circuit and a push-pull output stage, it accepts the output from the multiplexer 30A and outputs that to the first output port OUT1 of the integrated circuit 20 able to switch between ultrasonic and infrared carriers. When the enable signal ENZ1 36A is 0, the output buffer

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32A is in normal state, and when the enable signal ENZ1 36A is 1, the output buffer 32A is turned off and serves an output impedance.

The multiplexer [[24B]] 30B controls the output by use of a select control signal MODE2 34B. When the select control signal MODE2 34B is 0, the multiplexer 24B outputs the data signal DATA2 28B. On the contrary, when the select control signal MODE2 34A is 1, the multiplexer 24B outputs the inverse of the carrier FRE from the frequency divider 24 in combination with the inverter 26. The output buffer 32B accepts the output from the multiplexer 24B and outputs that to the second output port OUT2 of the integrated circuit 20 able to switch between ultrasonic and infrared carriers. When the enable signal ENZ2 36B is 0, the output buffer 32B is in normal state, and when the enable signal ENZ2 36B is [[0]] 1, the output buffer 32B is turned off and serves an output impedance.